

SDAC12-4

12-bit 4-channel DAC

User's Manual

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Section 7. Example Programs

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10 REM SDAC12-4 demonstration program. KH 871111
20 REM useful for setting up zero-offset and gain
100 base% = &2C0: dac% = base%+0
105 div%=63
110 mag = 1000
115 main
120 DEF main
200 WHILE 1
205 PRINT CHR$(26) :REM clear screen
210 PRINT " SDAC12-4 test programs: Main menu screen"
215 PRINT
220 PRINT " 1. minimum "
225 PRINT " 2. midrange "
230 PRINT " 3. maximum "
235 PRINT " 4. write any value "
245 PRINT " 5. set channel "
255 PRINT " 6. triangular wave "
260 PRINT " 7. sine and cosine waves"
265 PRINT " enter option ?"; INPUT option%
270 WHEN option%
275 IS =1 THEN wr_dac%(&000)
280 IS =2 THEN wr_dac%(&800)
285 IS =3 THEN wr_dac%(&FFF)
300 IS =4 THEN PRINT"digital value ? ";INPUT z%: wr_dac%(z%)
305 IS =5 THEN demo5
320 IS =6 THEN demo6
330 IS =7 THEN demo7
400 ENDWHEN
405 WEND
410 DEF wr_dac%(z%)
415 OUT dac%,hibyte%(z%): OUT dac%+1,lobyte%(z%)
420 DEF hibyte%(z%)
425 = ( (z% AND &FF00) /256 ) AND &00FF
430 DEF lobyte%(z%)
435 = z% AND &00FF
440 DEF demo5
450 PRINT "channel (0 to 3) ?": INPUT channel%
455 dac% = base% + 2* (3 AND channel%) : REM msb latch

```

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460 DEF demo6
465 WHILE 1
470   EXCLUDE SCAN
475   msb%=0
480   REPEAT                                     : REM start ramp upwards
510     OUT dac%, msb%: msb%=msb%+1           : REM latch msb
515     lsb%=0
520     REPEAT                                   : REM ramp lsb
525       OUT dac%+1, lsb%: lsb%=lsb%+1       : REM
530       UNTIL lsb% >= 255
535       UNTIL msb% >= 15
540     REPEAT                                   : REM ramp downwards
545       OUT dac%, msb%: msb%=msb%-1         : REM latch msb
550       lsb%=255                             : REM start of minor ramp
700     REPEAT
715       OUT dac%+1, lsb%: lsb%=lsb%-1
725       UNTIL lsb%=0
730       UNTIL msb%=0
735     INCLUDE SCAN
740   WEND

```

```

745 DEF demo7
750 x% = mag
755 WHILE 1
760   EXCLUDE SCAN
765   OUT(dac%+0), 8 + (x% AND &FF00)/256: OUT(dac%+1), x%
770   OUT(dac%+2), 8 + (y% AND &FF00)/256: OUT(dac%+3), y%
775   y% = y% + x%/div%
780   x% = x% - y%/div%
785   INCLUDE SCAN
790   WEND

```


Appendix A. Component List

Semiconductors

IC1	PAL22V10
IC2	LS244
IC3	LS240
IC4	LS688
IC5	LS244
IC6	LS175
IC7	LS164
IC8,11,14,17	AD7545
IC9,10,12,13	OP37
IC15,16,18,19	OP37
IC20	TL064
D1-8	IN4148
D9-12	LM385 Zener

Resistors

R1,4,7,10	15k
R2,5,8,11	10k
R3,6,9,12	4k7
R13-16	10k
R17,22,27,32	68R
R18,23,28,33	5k6
R19,24,29,34	12k
R20,25,30,35	12k
R21,26,31,36	3k3
R37	220R
RP1,3	4k7 x 8 SIL pack
RP2	4k7 x 7 SIL pack
VR1,3,5,7	2k0 multi-turn ceramic
VR2,4,6,8	2k0 multi-turn ceramic

Capacitors

C1-4,6-9	100 nF plate ceramics
C5,10,15,20	33 pF
C11-14,16-19	100 nF
C21,22,26-32	100 nF
C23	180 pF
C24,25,37	22 uF tant.
C33-36	33 pF

Appendix B. Connections

PL1. STEbus DIN41612 a/c row 64 way p.c.b. mounted plug

(for suitable backplanes refer to the current catalogue)

Pin	Row a c		
1	gnd	o o	gnd
2	+5v	o o	+5v
3	D0	o o	D1
4	D2	o o	D3
5	D4	o o	D5
6	D6	o o	D7
7	A0	o o	gnd
8	A2	o o	A1
9	A4	o o	A3
10	A6	o o	A5
11	A8	o o	A7
12	A10	o o	A9
13	A12	o o	A11
14	A14	o o	A13
15	A16	o o	A15
16	A18	o o	A17
17	CM0	o o	A19
18	CM2	o o	CM1
19	ADRSTB*	o o	gnd
20	DATAACK*	o o	DATSTB*
21	TRFERR*	o o	gnd
22	ATNRQ0*	o o	SYSRST*
23	ATNRQ2*	o o	ATNRQ1*
24	ATNRQ4*	o o	ATNRQ3*
25	ATNRQ6*	o o	ATNRQ5*
26	gnd	o o	ATNRQ7*
27	BUSRQ0*	o o	BUSRQ1*
28	BUSAK0*	o o	BUSAK1*
29	SYSCLK	o o	VSTBY
30	-12v	o o	+12v
31	+5v	o o	+5v
32	gnd	o o	gnd

There is one 50-way ribbon-cable header on the board, called PL2. It conforms to the standard I/O connection pattern, as set out below. It is intended that all A/D and D/A boards have this connector configuration, so that signal-conditioning boards are interchangeable.

PL2. 50-way p.c.b. mounted plug

(suitable ribbon-cable socket is RS 471-250)

+5V	50	o	o	49	+5V
+12V	48	o	o	47	-12V
D/A3	46	o	o	45	D/A2
D/A1	44	o	o	43	D/A0
n/c	42	o	o	41	GND
n/c	40	o	o	39	n/c
n/c	38	o	o	37	n/c
n/c	36	o	o	35	n/c
n/c	34	o	o	33	n/c
n/c	32	o	o	31	GND
n/c	30	o	o	29	n/c
n/c	28	o	o	27	n/c
n/c	26	o	o	25	n/c
n/c	24	o	o	23	n/c
n/c	22	o	o	21	GND
n/c	20	o	o	19	n/c
n/c	18	o	o	17	n/c
n/c	16	o	o	15	n/c
n/c	14	o	o	13	n/c
n/c	12	o	o	11	GND
Vin3	10	o	o	9	0V
Vin2	8	o	o	7	0V
Vin1	6	o	o	5	0V
Vin0	4	o	o	3	0V
GND	2	o	o	1	GND

Pins 13-40 are used for ADC inputs, and are not connected on this board. They are shown here for completeness.

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PL3. Test connector: 36-way p.c.b. mounted plug

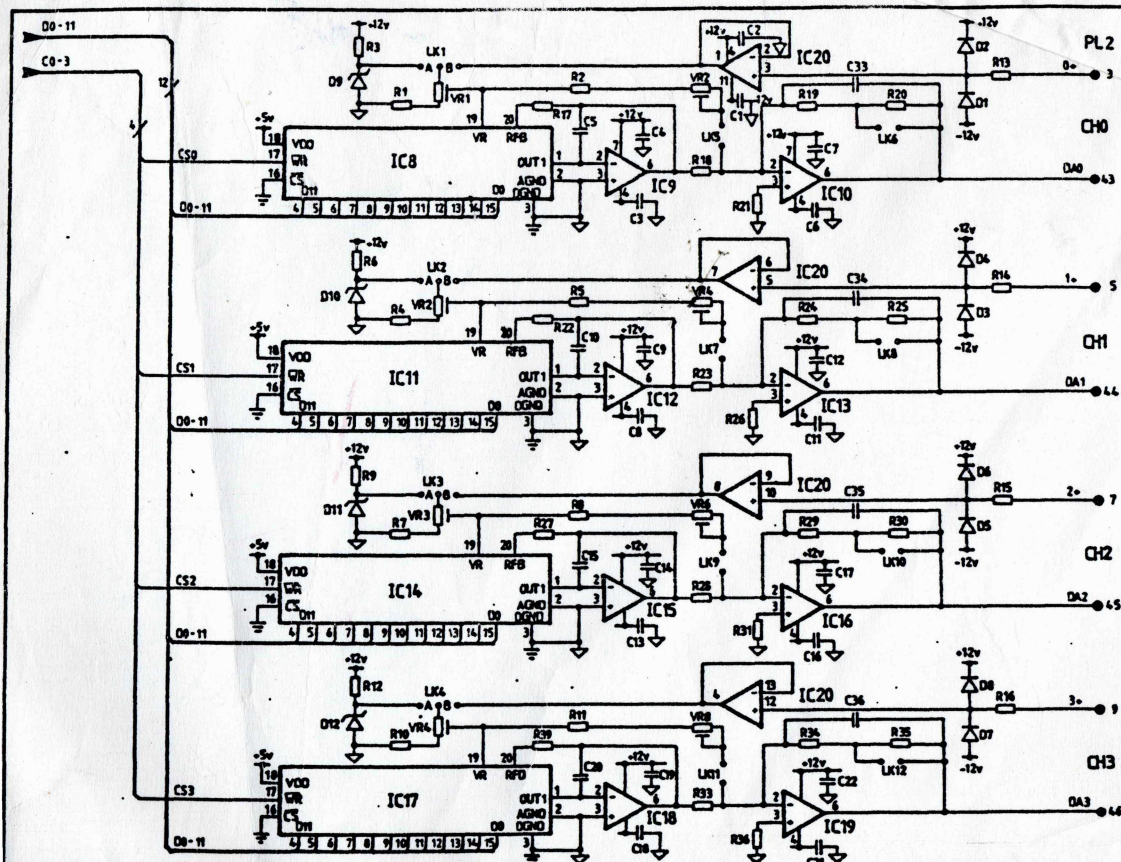
35 33 31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1

o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o

36 34 32 30 28 26 24 22 20 18 16 14 12 10 8 6 4 2

Appendix C. Specification

Operating temperature	5 C to 50 C (non-condensing)
Power consumption (typ)	5V +/- 0.25V 240mA 12V +/- 1V 60mA -12V +/- 1V 60mA
Output ranges	0 to 5V 0 to 10V +/- 2.5V +/- 5V
Input range	+/- 10V
Resolution	20mV/bit (adjustable)
Settling time	1.5 microseconds (typ)
Differential non-linearity	+/- 0.5 lsb (max)
Bus	STEBus
Bus connector	64a/c DIN 41612
Format	Single Eurocard
Dimensions	183mm x 100mm x 14mm
Weight	140g



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Title **SDAC 12-4**

Sheet 2 of 2

Drawing No **J130**

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